P2.15(d)

\[
\begin{align*}
[((xy)'x'((xy)'y)']' &= (xy)'x + (xy)'y \\
&= (x' + y')x + (x' + y'y) \\
&= xx' + xy' + x'y + y'y \\
&= xy' + x'y \\
&= x \oplus y
\end{align*}
\]

P3.27.

(a) \[F = x'y + xy'
\]

(b) \[F = w'x' + wyz + wy'z' + wy'z
\]

(c) \[F = wy'y + wx'y'
\]
When taking the previous bit-slice into consideration, \((x_i \geq y_i)\), can be a 1 only if the previous \((x_i \geq y_{i-1})\) is also a 1.

**NOTE:** This doesn’t work!

We can construct a 4-bit iterative comparator circuit using the 1-bit comparator circuit for \((x_i \geq y_i)\) from P.4.28.
P7.8.

State diagram:

Next-state (Implementation) table:

<table>
<thead>
<tr>
<th>Current State $Q_1, Q_0$</th>
<th>Next State $Q_{next}, Q_{next}, (D_1, D_0)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00, 00, 11, 01</td>
</tr>
<tr>
<td>01</td>
<td>00, 01, 01, 11</td>
</tr>
<tr>
<td>10</td>
<td>10, 10, 01, 11</td>
</tr>
<tr>
<td>11</td>
<td>11, 11, 10, 00</td>
</tr>
</tbody>
</table>

Excitation equations:

$D_1 = \text{Count}'Q_1 + \text{Count}(\text{Up} \oplus Q_1 \oplus Q_0)'$

$D_0 = \text{Count}'Q_0 + \text{Count}Q_0' = \text{Count} \oplus Q_0$

Diagram of the circuit.