Integrated Circuit (IC) Fabrication

The beginning …

What are Integrated Circuits?

- Electrical components (transistors, resistors, capacitors, etc.).
- Combine basic components into more complex electrical devices (amplifiers, multiplexers, analog-to-digital converters, etc.).

Photo courtesy of Intel Corporation.

Intel Pentium Microprocessor Chip
Typical Materials Used

- Single crystal silicon – SCS
  - Semiconductor, good heat conductor
- Polycrystalline silicon – “polysilicon”
  - Mostly isotropic material, also semiconductor
- Silicon dioxide – SiO$_2$
  - Good thermal and electrical insulator
  - Thermal oxide, LTO, PSG: different names for different deposition conditions and methods
- Aluminum – Al
  - Metal, thermal and electrical conductor
- Silicon nitride – Si$_3$N$_4$
  - Excellent electrical insulator

Silicon Wafer Manufacturing

Single crystal silicon “boule” is pulled out of the spinning melt. Pulling speed defines boule diameter.

Reference: www.egg.or.jp/MSiL/english/index-e.html
**Typical Design Process**

- **Idea, circuit concept**
- **Computer Aided Design (CAD)**
  - Draw device in 2D (top view) = “layout”
  - Fabrication design rule checking
- **Simulation**
  - Circuit extraction based on layout
  - Electrical device models
  - Electrical circuit simulation to verify functionality
- **Create masks for fabrication**
  - Output of CAD program is GDSII or CIF files for mask generation

**Computer Aided Design (CAD)**

- Draw in 2D, top view
- Component libraries
- Automatic, real-time design rule checking
- Output = GDSII or CIF files for mask generation
Photomask for Fabrication

- Typically a layer of chrome patterned on glass plate.
- One mask for each deposition and etch step.

Photos courtesy of Photronics, Inc.

Photolithography

Microscale pattern transfer
Ion Implantation

Altering the substrate …
Selecting “Dopants”

III A
B
Boron

IVA
Si
Silicon

VA
P
Phosphorus

“P-type”

“N-type”

Ion Implanter

Ion source

Acceleration tube (high voltage)

Analyzer magnet (to select desired species)

Acceleration and beam focusing

Silicon substrate

Diagram courtesy of Case Technology, Inc.
Ion Implantation

- High voltage (up to 175 keV) is used to accelerate a beam of impurity ions towards the silicon surface, penetrating the surface.
- Possible mask (barrier) materials = photoresist, silicon dioxide, silicon nitride, aluminum, etc.
- Source and drain regions in CMOS transistors formed by ion implantation.

Thin Film Deposition

Adding to the substrate …
How are films applied to the substrate?

- Thermal oxidation (SiO₂)
- Chemical Vapor Deposition (CVD)
  - Low Pressure CVD (LPCVD)
  - Plasma Enhanced CVD (PECVD)
  - Polysilicon, silicon nitride, dielectrics
- Evaporation (metals)
  - Thermal evaporation
  - E-beam evaporation
- Sputtering (metals, dielectrics)
- Spin-on & Cure

Thermal Oxidation of Silicon

- Not really an application process but a growth process.
- Two methods: wet (atmosphere contains water vapor) and dry (atmosphere contains pure O₂ gas). Oxygen arriving at the surface combines with silicon to form SiO₂.
- High temperature process: 900 – 1200°C
- Requires dedicated quartz furnaces.
**Low Pressure CVD**

- Chemical reaction of gaseous compounds forms a thin film on wafer surface.
- Deposition temp = 600 – 1150°C
- Pressure = 30 – 250Pa
- Excellent film uniformity and conformal coverage
- Appropriate gases used to deposit polysilicon, SiO₂, silicon nitride, tungsten.

**Plasma Enhanced CVD**

- RF signal between top & bottom electrodes (wafers) creates plasma.
- The chemical bonds of the gases are broken – solid precipitates form a thin film on the wafer surface
- Lower temperature deposition compared to LPCVD (400°C or less)
- Higher deposition rate compared to LPCVD
- Can deposit SiO₂, silicon nitride, amorphous Si.
**Metal Evaporation**

**Vacuum chamber**

- Metal source is melted and evaporates. Gas molecules form a film on the wafer surface.
- Under vacuum, mean free path of gas molecules is large.

**Thermal Evaporation**

- Loops of metal wire are hung from a tungsten filament.
- By heating the filament, the metal melts and wets the filament.
- Further heating evaporates the metal from the filament.

- Alternatively, pellets of metal can be loaded into a tungsten boat.
- Heating the boat melts and evaporates the metal.
- Line-of-sight deposition.
E-Beam Evaporation

- Evaporate metals & dielectrics (SiO₂)
- High vacuum required (10⁻⁷, 10⁻⁸ Torr)
- Line-of-sight deposition.
- Need internal wafer rotation for better step coverage.

Step Coverage Problem

Totally shadowed region
Deposition via Sputtering

- Argon plasma knocks atoms off target
- Ejected material travels to the substrate, creating a film
- Metals need a DC power supply
- Dielectrics (SiO₂, AlOₓ) need RF power supply (13.56 MHz)
- Greater uniformity control, better step coverage

Spin Casting and Curing

- Viscous liquid is poured on center of wafer
- Wafer spins at 1000-5000 RPM for ~30s
- Baked on hotplates 80-500°C for 10-1000sec, or cured in oven
- Deposition of polymers, photoresist, sol-gel precursors
Thin Film Etching

How are films patterned on the substrate?

- Photolithography followed by:
  - Wet Etching
  - Dry Etching
- In the case of metals, can also do “lift-off.”
**Example: Metal Patterning**

- **Mask**
- **Metal**
- **Silicon**

**Wet etching**

- **“Lift-off”**

**Dry Etch: Reactive Ion Etching (RIE)**

- **Mask**
- **Silicon**
- **Substrate**

**Pre-Etch**

**Etch**

**Typical gases used:** $O_2$, $SF_6$, $CF_4$

- For silicon etching: $CF_4 + O_2$

Drawing courtesy of G. O'Brien, U. Michigan
CMOS Integrated Circuits

- MOSFET = Metal Oxide Semiconductor Field Effect Transistor
- NMOS = N-channel MOSFET, PMOS = P-channel MOSFET
- CMOS IC = Complementary Metal-Oxide-Semiconductor Integrated Circuit (i.e. combines both NMOS and PMOS transistors into a single circuit).

**NMOS transistor**

- Aluminum interconnect
- Gate (polysilicon)
- Insulation ($SiO_2$)
- Source
- Drain
- N-type ion implanted regions
- Conducting n-type region forms here when gate is brought positive

**PMOS transistor**

- Silicon substrate
- P-type ion implanted region